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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/~~792,822~~ 729882
Filing Date	12/12/2000
First Named Inventor	Cotteverte, et al
Group Art Unit	1765
Examiner Name	Robert K. Kunemund
Total Number of Pages in This Submission: 51	Attorney Docket Number: Cotteverte 2

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
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- ☐ Certified Copy of Priority Document(s)
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Corning Incorporated, SP-TI- 3-1, Corning, NY 14830
Signature	Walter M. Douglas
Date	13 August 2003

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	J.C. Cotteverte et al.
Serial No:	09/729,822
Filing Date:	December 5, 2000
Title:	METHOD FOR MAKING AN INTEGRATED OPTIAL CIRCUIT

Examiner: Robert K. Kunemund

Group Art Unit: 1765

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants respectfully submit this Brief to the Board of Patent Appeals and Interferences to appeal the final rejection dated March 20, 2003, of the above identified application. Appellants filed the Notice of Appeal on June 18, 2003, and now submit this Brief in triplicate, as required by 37 C.F.R. § 1.192(a). Appellants have also filed the appropriate petition and paid the required fee to gain an extension of the due date for filing this Brief to the Board. Please charge Deposit Account Deposit Account No. 03-3325 the $320.00 fee under 37 CFR 1.17(c) for filing the Appeal Brief. If any extension of time under 37 C.F.R. § 1.136 is required to make the submission of this Appeal Brief timely, such an extension is requested and the fee should also be charged to our Deposit Account No. 03-3325.

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Corning Incorporated.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-3 and 5-25 remain in the application. These are the pending claims that are the subject of this Appeal and are set forth in the attached Appendix. Claim 1 has been amended twice. Claim 4 was cancelled in Appellants Response to the Final Office Action filed on May 19, 2003.

IV. STATUS OF AMENDMENTS

Appellants received an Advisory Action mailed May 30, 2003 advising: (1) that the 35 U.S.C. §112, first paragraph, rejection was overcome; (2) that all claims remain rejected (under 35 U.S.C. §§ 102 and 103); and (3) that the last amendments to the claims would be entered for purposes of Appeal. Accordingly, in this Brief Appellants' reference to the claims 1-3 and 5-25 remaining in the application refer to the claims as of May 19, 2003. A complete set of claims 1-3 and 5-25 is attached hereto.

V. SUMMARY OF INVENTION

The present invention relates to a method for manufacturing an integrated optical circuit in which an optical device (for example, a waveguide, resonator, etc.) is associated with an array structure (for example, a frequency band gap region). In particular, the method comprises:

- forming on a face of a substrate a first mask that defines a pattern corresponding to at least one optical device to be formed in a first region of the substrate;
- forming on the face of the substrate a second mask defining a pattern corresponding to an optical structure to be formed in a second region of the substrate distinct from the first region; and
- etching the substrate having thereon the first and second masks in order to form the at least one optical device and the optical structure on the substrate.

Utilizing the foregoing method one is able to produce in a single step an integrated

optical structure on a substrate in accordance with the patterns set by the two masks. The patterns defined by the two masks are distinct from one another as set forth in claim 1 and in the specification at page 3, lines 10-16.

The novel feature of the invention is that the two masks are used simultaneously to produce an integrated optical circuit having different elements in different regions of a substrate in a simplified manner thus reducing costs. In addition, the method allows one to produce an integrated circuit with great accuracy. This is particularly important in the productions of integrated telecommunications circuits utilizing photonic crystals.

An example of such an integrated circuit is one have one or more optical devices such as waveguides, couplers, splitters and so forth, and an array structure such as one defining a photonic band gap proximate to the optical device. In such integrated circuits the optical device(s) and the array structure have quite different shapes. For example, the array structure may be periodic or quasi-periodic with a period that may be small (for example, ca. 200-250nm) whereas the device is not. A typical technique to prepare a mask suitable for making such periodic structure is interference lithography which uses two interfering laser beams. However, interference lithography is not suitable for forming a mask corresponding to optical devices (e.g., waveguides, couplers, etc.) because such devices do not consist of a periodic or quasi-periodic structure. These masks must be produced using a more conventional lithographic technique such as irradiation by UV (ultraviolet) light.

According to the invention one forms two different masks on a substrate. Each mask is directed to a different region of the substrate and is use to for different elements as described above. Once the masks are formed on the structure, a single technique such as etching can then be used to form the integrated circuit.

In contrast to the present invention, using a single mask for both an optical device and an optical structure would require a complicated lithographic method for producing the mask. Such method would have to be adapted to all the different types of shapes contained in the pattern to be created in the substrate. While the known UV and electron beam lithographic techniques are suitable for producing masks for waveguides, couplers and similar devices, at the present time they do not have sufficient accuracy for form array structures such as the photonic band gap mentioned above. Consequently, a better method as exemplified by the present invention is required

VI. ISSUES

Issues presented for consideration in this Appeal are:

A. Whether claims 1-3 and 5-25 are patentable under 35 U.S.C. §102 (b) as not being anticipated by U.S. Patent No. 5,049,978 to Bates et al. (hereinafter "Bates").

B. Whether claims 1-3 and 5-25 are patentable under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,049,978 to Bates et al. (hereinafter "Bates").

C. **NOTE:** Claim 1-25 were also rejected in the Final Office Action under 35 U.S.C. §112, first paragraph. However, this rejection was withdrawn in the Advisory Action issued in response to Appellants response after the Final office Action in which appellants entered amendments. Accordingly, since the Examiner indicated in the Advisory Action that amendments would be entered for purpose of appeal, the §112, first paragraph, rejection is not discussed herein.

VII. GROUPING OF CLAIMS

In compliance with 37 C.F.R. § 1.192(7), Appellants state that all of the claims stand or fall together. Claim 1 is the only independent claim in the application. Claims 2-3 and 5-25 depend on claim 1.

VIII. ARGUMENTS

A. The Examiner's Rejection. Claims 1-3 and 4-25

In the Final Office Action of March 30, 2003, the Examiner rejected pending claims 1-3 and 5-25 under 35 U.S.C. §102(b) as anticipated by, or in the alternative under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,049,978 to Bates et al.]. On pages 3 and 4 of the final Office Action, the Examiner stated that:

> "The Bates et al reference teaches a conductively enclosed hybrid assembly. A substrate of silicon is provided (column 4, lines 38-42). Recesses are created in the substrate. A preferred etches [*sic*] for creating the recesses in the silicon substrate is plasma etch. The etch is patterned by a metal such as Cr, TiW, Ti, or Al. A first step in mask formation is the sputtering of an unpatterned metal of the plasma resistant metal covering the upper surface of the substrate (col 5, lines 15-21). This reads of the first masking step. The metal layer is then

patterned. The metal layer is covered with a photoresist, which is exposed to an optical pattern defining the recesses. The claimed second masking step. The region of the metal layer from which the photoresist has been removed are then exposed to an acid etch to create openings in the metal mask (col 5, lines 29-34). A solvent may remove the photoresist. The recesses support individual MMIC chips. The use of a silicon substrate has the further advantage of permitting efficient optical interconnection with optical circuits within the package while maintaining a hermetic seal col 13, lines 15-20. The Bates et al reference does not teach that an optical device is formed in the first and second region of the substrate. However, the Bates et al. Reference teaches that MMIC chips are formed in the recess in the substrate. MMIC chips are optical devices. Thus it would have been obvious to one of ordinary skill in the art that Bates et al inherently teaches optical devices are formed in the substrate." [*Sic.*]

Applicant respectfully submits that the Examiner failed to provide a *prima facie* case of either anticipation or obviousness because:

(a) With regard to anticipation, Bates does not teach the formation of two masks defining "a first and second pattern in distinct regions". Anticipation requires that a single reference teach each and every element of the claimed invention be present in the cited art as will be shown below, this does not occur in the Bates patent. I

(b) With regard to obviousness, one of ordinary skill in the art would not be motivated to use or modify the teaching of Bates to obtain Applicant's invention because Bates neither teaches nor suggests that one can use two masks defining separate patterns. In re Vaeck, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

B. Appellant's Argument

The claimed invention is best understood by a review of the steps of Bates and comparing them with those of the claimed invention. While the Examiner attempted to summarize Bates in Section VIII A above, Appellants believe that summary is defective because it does not properly describe what Bates actually does. It is here noted that what Bates is seeking to do is to make recesses in the substrate into which MMIC chips, made elsewhere, can be inserted and subsequently bonded to a metallic layer. Bates does not use two masks to simultaneously form two different elements, for example a device and an array, on the surface of a substrate.

Where necessary to fully explain what is being taught, Appellants have entered and identified their comments.

(1) What Bates teaches is:

1. Providing a substrate (column 4, lines 38-42) into which the recesses are to be formed.
2. Applying an unpatterned metal layer to the substrate (column 5, lines 19-20).

   • **Appellants' Comment:** While one may argue that this layer is a mask, at this point it is unpatterned and defines no element or device in a distinct region of the substrate.
3. Covering the metal layer with a photoresist and subjecting the photoresist to an "optical pattern" that defines the recesses that are to be formed in the substrate (column 5, lines 22-24).

   • **Appellants' Comment:** The patent does not specify whether the "optical pattern" is in the form of a mask that is applied to the photoresist or is an image project onto the photoresist. Whichever the case may be, there are not two different patterns defining different areas of the substrate.
4. The photoresist is chemically developed and the polymerized area of the photoresist removed to expose the underlying metal layer (column 5, lines 24-29).

   • **Appellants' Comment:** At this point there is a single mask defining a single pattern; namely, photoresist layer having a part thereof removed to define the recesses that are to be made.

5. The metallic layer is then wet etched to remove the exposed metal and bare the substrate (column 5, lines 29-32). The undeveloped photoresist may then be removed (column 5. lines 32-34).

   • **Appellants' Comment:** The Examiner has argued that after the wet etching there are two masks present on the substrate, one being the photoresist layer and the other being the metal layer. However, In Bates both define the same pattern in the same regions of the substrate and not different patterns in distinct regions of the substrate as Appellants are claiming.

6. After wet etching the patterned metal mask is subjected to a plasma etch to form the recesses in the substrate (Bates, column 5, lines 35-43).

7. When the plasma etching is completed and the recesses are formed the metal mask is removed (column 5, lines 56-57). The substrate surface is cleaned and metalized with (1) chromium, (2) nickel and (3) gold. The MMIC chips are then inserted into the recess and bonded to the gold layer.

   • **Appellants' Comment:** The MMIC chips are formed elsewhere, inserted into the recesses and bonded to the gold layer. The MMIC chips are not formed in the substrate as the Examiner has stated in the Final Office Action. (See Bates, (See column 3, lines 1-9 and column 6, lines 2-5, both of which indicate that the MMIC chips are inserted into the substrate and bonded to a metallic layer.) Consequently, Appellants submit that the Examiner conclusion that Bates teaches the formation of optical devices in a substrate is erroneous.

In contrast to Bates, Appellants teach and claim a method for the formation of two separate "elements" in different regions of a substrate. The substrate is then etched in a single step and the two elements are formed as a result on this single etching step. Appellants steps are as follows. A copy of Appellents' Figures reference below is attached as Appendix B.

(2) What Appellants teach and claim.

1. A metal layer 8 and a first photoresist 9 are applied to a substrate 7. Substrate 7 consists of a silica base substrate 7a, a first thin silica layer 7b and a second thin silica layer 7c on top of layer 7b, where the refractive

index of 7c is higher than that of 7b. (See the application, page 7, lines 22-28).

2. A silica mask, having a chromium pattern on its upper surface defining an optical waveguide to be formed in the substrate, is placed over to the photoresist layer 9 and resulting masked substrate exposed to UV radiation (application, page 7, line 29 to page 8, line 7).
3. The silica mask is removed and the photoresist layer 8 developed leaving only a portion of the photoresist layer 9a (Fig. 2C) having the same shape as the chromium pattern (application, page 8, lines 8-12).
4. The metal layer 8 is then wet etched to remove the metal not covered by the photoresist remaining on the substrate (application, page 8, lines 13-19). As a result of the wet etching the photoresist is them removed (application, page 8, lines 19-20). To form a metal mask 8a defining a pattern, in this case being a waveguide.
5. A second photoresist layer 11 is formed on substrate 7 and metal mask 8a (application, page 8, lines 21-27, and Fig. 2F).
6. Two interfering lasers are directed to the photoresist 11 to form a pattern such that after development of the photoresist a second pattern is formed, in this case the mask defining an array of holes to be formed. (See application, page 8, line 28 to page 9, line 5).

   Appellants' comment: **<u>As per claim 1 and the specification on page 9, lines 5-6, at this point there are two masks present on the substrate.</u>** These masks define different elements in different regions of the substrate. One is the waveguide and the second is the array. Both the photoresist and metal masks are resistant to dry etching (application, page 9, lines 6-7)
7. A dry etch is performed without eroding the two masks (application, page 9, lines 8-13).
8. The masks are removed to leave a waveguide and an array on the substrate (application, page 9, lines 14-22).

   Appellants' comment: Note that Appellants do not require the insertion of a separately formed device into the substrate as is required by Bates.

Appellants submit that the above comparison clearly indicates that the Bates

patent does not teach the claimed invention. Bates does not teach the simultaneous use of two masks defining two different elements and/or devices in different regions of a substrate in a single forming step. There is no suggestion in Bates that such a procedure can be used. What Bates does do is form a recess in a substrate into which a device formed independently, the MMIC chip, can be inserted.

IX. CONCLUSION

In conclusion, in view of the comparisons, facts and arguments set forth above Appellants request requests a reversal of each of the grounds of rejection maintained by the Examiner and submit that the application and claims therein are allowable.

If there are any other fees due in connection with the filing of this Brief on Appeal, please charge the fees to our Deposit Account No. 03-3325. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for herein, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

By: Walter M. Douglas Date: 13 August 2003

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Walter M. Douglas 13 Aug 2003
Walter M. Douglas (Signature) DATE

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The claims on appeal are as follows:

1. (previously amended) A method for manufacturing an integrated optical circuit on a substrate, the substrate having a first region and a second region distinct from the first region, the method comprising the steps of:

forming a first mask on the substrate, the first mask defining a pattern corresponding to at least one optical device to be formed in the first region of the substrate;

forming a second mask on the substrate, the second mask defining a pattern corresponding to an optical structure to be formed in the second region of the substrate; and

etching the substrate having simultaneously thereon the first and second masks in order to form the at least one optical device and the optical structure on the substrate,

wherein said etching comprises using a predetermined etching gas, and said first and second masks are made of a material which substantially resists the predetermined etching gas..

2. The method of claim 1 further comprising the step of:

removing the first mask and the second mask.

3. The method of claim 1 wherein the step of etching is dry etching using a predetermined etching gas.

4. (cancelled)

5. The method of claim 3 wherein the predetermined etching gas is a fluorine-bearing gas.

6. The method of claim 1 wherein the steps of forming the first mask and the second mask are carried out such that the first mask and the second mask overlay one another.

7. The method of claim 6 wherein the first mask has a first portion which overlays the second mask and a second portion which is in direct contact with the substrate.

8. The method of claim 1 wherein one of the first mask or the second mask is formed using an interference lithography technique and the other of the first mask or the second mask is formed using a UV exposure technique.

9. The method of claim 1 wherein the second mask is formed using an interference lithography technique and radiation, and the first mask is made of a material which is substantially insensitive to the radiation used in the interference lithography technique, so that the second mask may be formed after the formation of the first mask without affecting the first mask.

10. The method of claim 9 wherein the step of forming the second mask comprises the steps of :

forming a photoresist layer on the substrate; and

forming a pattern corresponding to the optical structure in the photoresist layer using the interference lithography technique.

11. The method of claim 9 wherein the first mask is made of a metal and the second mask is made of a photoresist material.

12. The method of claim 11 wherein the first mask is made of a metal selected fom the group consisting of nickel, chromium, or gold.

13. The method of claim 9 wherein the step of forming the first mask comprises the steps of :

forming a first layer on the substrate, the first layer being made of a material which is substantially insensitive to light;

forming a photoresist layer on the first layer;

patterning the photoresist layer using the UV exposure technique to obtain a photoresist pattern corresponding to the first region of the substrate;

etching the first layer using the photoresist pattern as the first mask; and

removing the photoresist pattern.

14. The method of claim 13 wherein the step of etching the first layer is wet etching.

15. The method of claim 9 wherein the first mask and the second mask are both made of a photoresist material, the first mask being a photoresist material which has been heated to remove its sensitivity to light.

16. The method of claim 15 wherein the step of forming the first mask comprises the steps of:

forming a photoresist layer on the substrate;

patterning the photoresist layer using a UV exposure technique to obtain a pattern corresponding to the first region of the substrate; and

heating the photoresist pattern to remove its sensitivity to light.

17. The method of claim 1 wherein the first mask is formed using a UV exposure technique and the second mask is made of a material which is substantially insensitive to UV radiation, so that the first mask may be formed after the formation of the second mask without affecting the second mask.

18. The method of claim 1 wherein the substrate is a silicon on insulator substrate.

19. The method of claim 1 wherein the optical structure is an array structure.

20. The method of claim 1 wherein the second region of the substrate is proximate to the first region.

21. The method of claim 20 wherein the array structure consists of a periodic array of irregularities.

22. The method of claim 21 wherein the array structure defines a frequency band gap.

23. The method of claim 21 wherein the array structure is a periodic array of holes.

24. The method of claim 21 wherein the array structure is a periodic array of rods.

25. The method of claim 21 wherein the at least one optical device is a waveguide.

APPENDIX B TO BRIEF ON APPEAL

Figures 2A-2J referred to in the Brief are shown on the following pages.

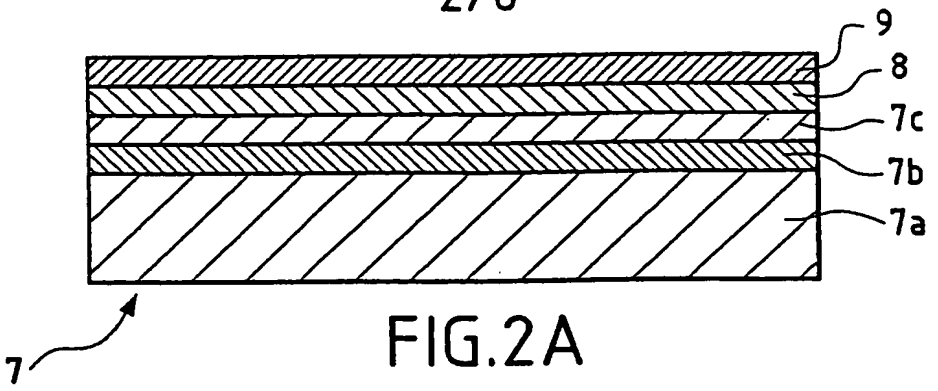

FIG.2A

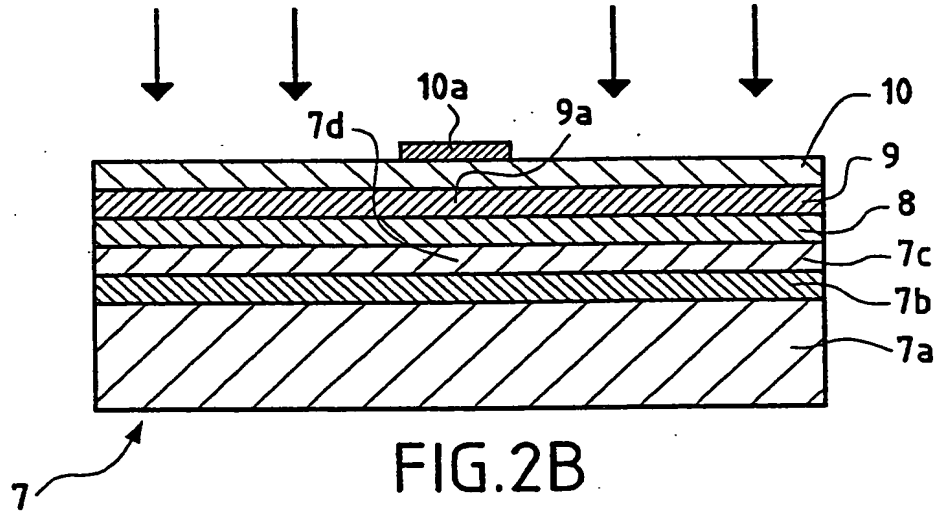

FIG.2B

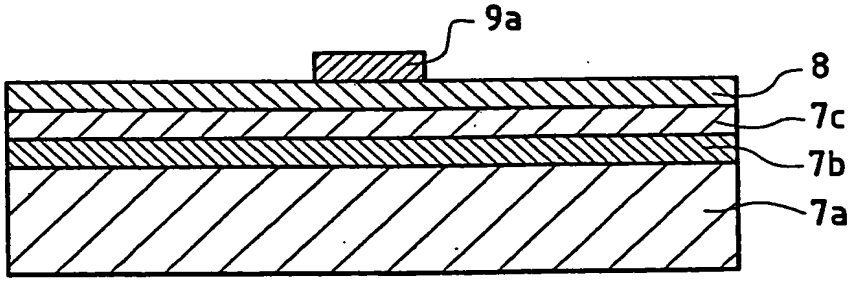

FIG.2C

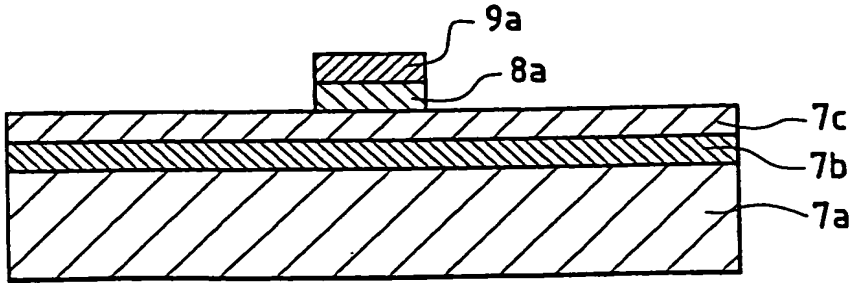

FIG.2D

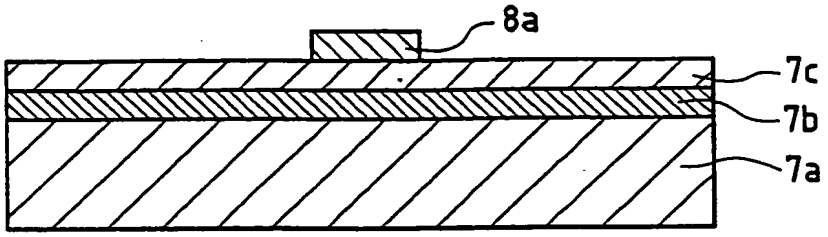

FIG.2E

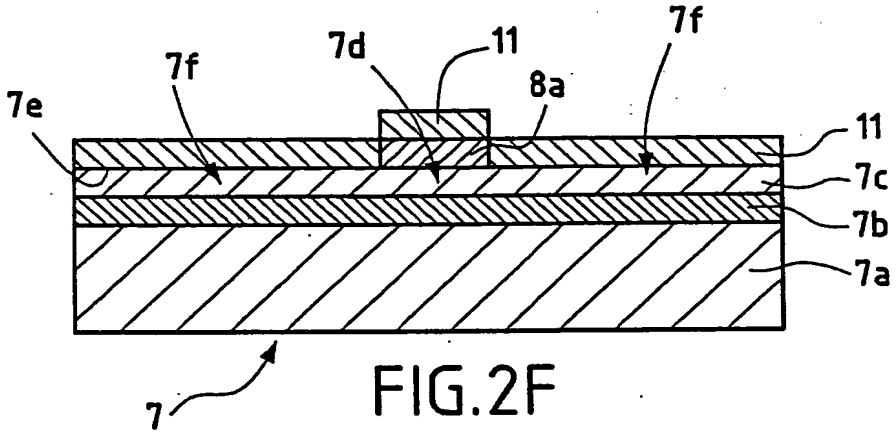

FIG.2F

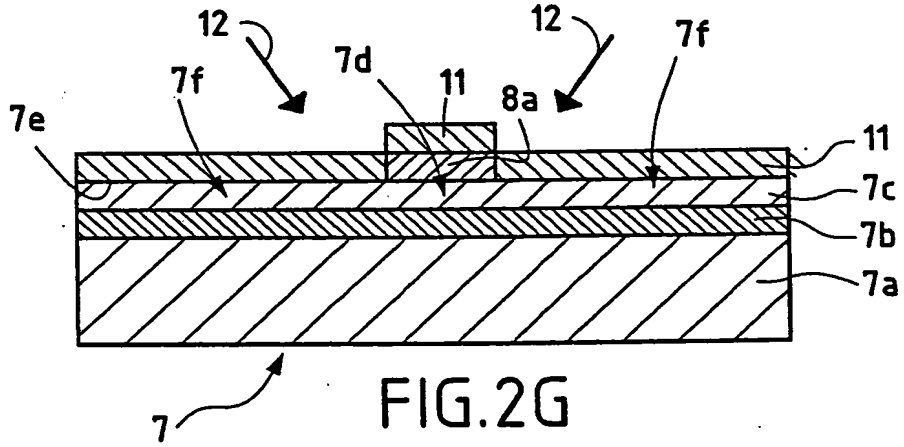

FIG.2G

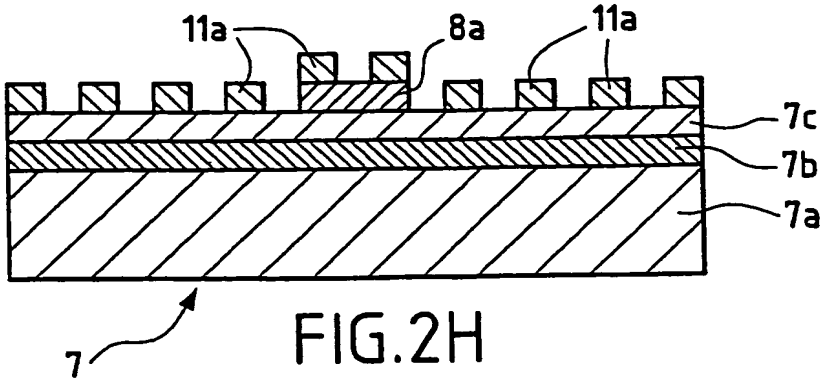

FIG.2H

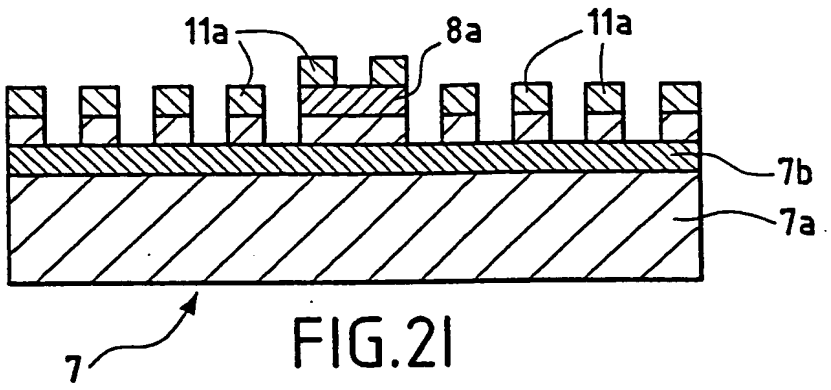

FIG.2I

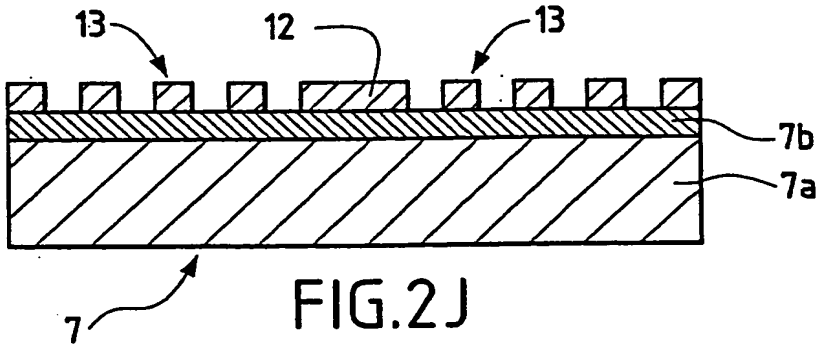

FIG.2J

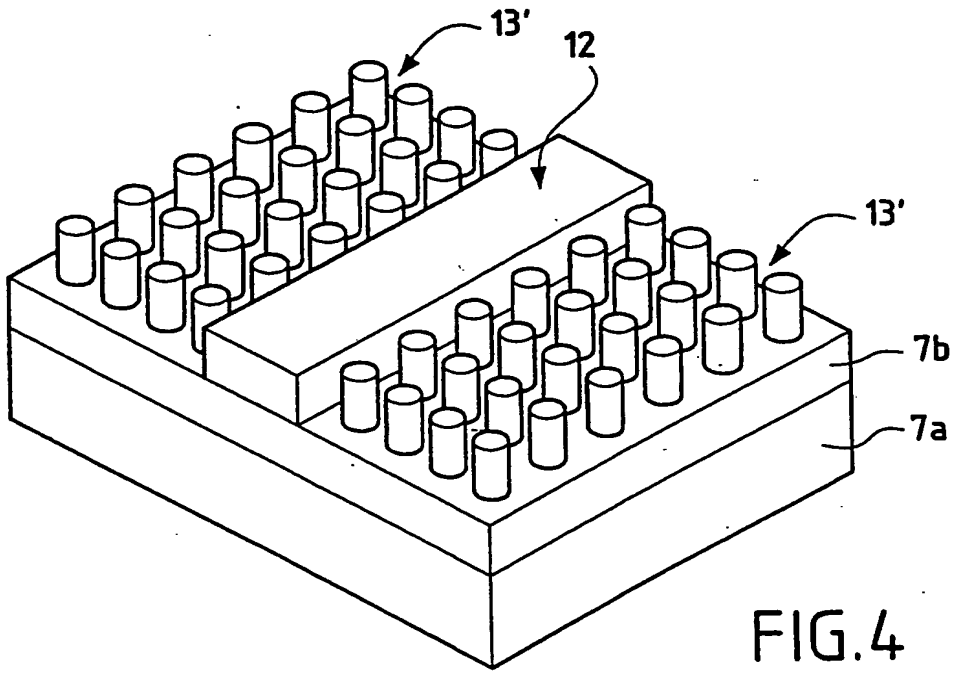

FIG.4